What is claimed is:

1. A computer comprising:

a controller which executes a reset process, in response to a reset signal;

an oscillator oscillates a clock; and

a timer which counts pulses of the clock, and outputs the reset signal to said controller, in a case where a counted value obtained by counting the pulses of the clock exceeds a predetermined limit value; and

wherein said controller controls said timer, and clears the counted value before the counted value exceeds the limit value, and

said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process.

2. The computer according to claim 1, wherein

said timer has a plurality of operational modes.

3. The computer according to claim 2, wherein:

said controller outputs a mode specification signal for specifying an operational mode of said timer, to said timer; and

said timer sets an operational mode thereof, in accordance with the mode specification signal.

4. The computer according to claim 3, wherein

said timer includes a circuit, which sets the mode specification signal sent from said controller ineffective in response to setting of the operational mode of said timer.

5. The computer according to claim 3, wherein

said timer further includes a restriction circuit which restricts an allowable period of time the mode specification signal provided from said controller can be accepted.

6. The computer according to claim 4, wherein

said timer further includes a restriction circuit which restricts an allowable period of

time the mode specification signal provided from said controller can be accepted.

7. A watchdog timer comprising:

a counter which counts pulses of a clock generated by an oscillator, and clears a counted value of the pulses, in response to a clear signal for designating to clear the counted value and being supplied from an external circuit; and

an output circuit which outputs a reset signal for designating to execute a reset process to said external circuit, in a case where the counted value exceeds a predetermined limit value, and

wherein said counter clears the counted value and begins counting the pulses of the clock in response to the reset signal output from said output circuit, thereby detecting an abnormal operation occurring in said external circuit during execution of the reset process.

8. The watchdog timer according to claim 7, wherein

said watchdog timer has a plurality of operational modes.

9. The watchdog timer according to claim 8, further including

a mode setting circuit which sets an operational mode of said watchdog timer, in accordance with a mode specification signal which specifies the operational mode and is provided from said external circuit.

10. The watchdog timer according to claim 9, further including

a circuit which sets the mode specification signal sent from said external circuit ineffective, in response to setting of the operational mode of said watchdog timer.

11. The watchdog timer according to claim 9, further including

a restriction circuit which restricts an allowable period of time the mode specification signal provided from said external circuit can be accepted.

12. The watchdog timer according to claim 10, further including

a restriction circuit which restricts an allowable period of time the mode specification signal provided from said external circuit can be accepted.

13. An abnormal operation detection method comprising:

counting pulses of a clock generated by an oscillator;

clearing a counted value of the pulses, in response to a clear signal which is provided from an external circuit and designates to clear the counted value; and

controlling said external circuit to execute a reset process, in a case where the counted value exceeds a predetermined limit value, and

wherein said counting includes detecting an abnormal operation occurring in said external circuit during execution of the reset process, by counting the pulses of the clock in synchronization with that said external circuit begins the reset process.

14. The detection method according to claim 13, wherein

said detection methods includes a plurality of modes.

15. The detection method according to claim 14, further including

setting a mode of the detection method, in accordance with a mode specification signal which is provided from said external circuit and specifies the mode.

16. The detection method according to claim 15, further including

setting the mode specification signal which is provided from said external circuit ineffective, in response to setting of the mode.

17. The detection method according to claim 15, further including

restricting an allowable period of time the mode specification signal provided from said external circuit can be accepted.

18. The detection method according to claim 16, further including

restricting an allowable period of time the mode specification signal provided from said external circuit can be accepted.